AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all previous listings of claims in the present application.

What is Claimed is:

1. (Currently Amended) A redundancy control circuit comprising:

a plurality of program elements, in which a defect address indicating a position of a defect is programmed by a dielectric breakdown due to applying of a voltage; and

a voltage control section which applies said voltage to part of a plurality of targeted program elements simultaneously,

wherein said plurality of targeted program elements is part of said plurality of program elements to be dielectrically broken down correspondingly to said defect address, and

wherein said voltage control section includes a timing setting section which outputs a timing signal indicating a timing for carrying out a dielectric breakdown of each of said plurality of program elements based on a trigger signal.

2. (Currently Amended) The redundancy control circuit according to claim 1, wherein:

a number of said part of the plurality of targeted program elements, of which number is less than a number of said plurality of program elements, is one, and

said voltage control section applies said voltage to each of said plurality of targeted program elements, one by one.

3. (Original) The redundancy control circuit according to claim 1, wherein said voltage control section applies said voltage to said plurality of targeted program elements, at a timing of a trigger signal.

4. (Original) The redundancy control circuit according to claim 1, wherein said voltage control section commonly applies said voltage to said plurality of targeted program elements, and

said voltage is a voltage generated inside a device including said redundancy control circuit.

5. (Currently Amended) The redundancy control circuit according to claim 1, wherein said voltage control section further includes:

~~a timing setting section which outputs a timing signal indicating a timing for carrying out a dielectric breakdown of each of said plurality of program elements based on a trigger signal, and~~

a plurality of element breakdown sections, each of which is installed correspondingly to said each of the plurality of program elements and applies said voltage to corresponding one of said plurality of program elements based on said timing signal and said defect address.

6. (Original) The redundancy control circuit according to claim 5, wherein each of said plurality of element breakdown sections includes:

a fuse breakdown setting section which applies a specifying signal at a timing of said timing signal based on said defect address, wherein said specifying signal indicates whether or not said corresponding one of the plurality of program elements should be dielectrically broken down, and

a voltage applying section which applies said voltage to said corresponding one of the plurality of program elements in responses to said specifying signal, when said specifying signal indicates that said corresponding one of the plurality of program elements should be dielectrically broken down.

7. (Original) The redundancy control circuit according to claim 6, wherein a first timing is different from a second timing,

said first timing is a timing when a first said fuse breakdown setting section for a first one of said plurality of program elements, outputs a first said specifying signal, and

said second timing is a timing when a second said fuse breakdown setting section for a second one of said plurality of program elements, outputs a second said specifying signal.

8. (Previously Presented) The redundancy control circuit according to claim 7, further comprising:

a comparing section which compares said voltage with a standard voltage and outputs a comparing result signal,

wherein said timing setting section generates said second timing based on said trigger signal and said comparing result signal indicating that said voltage exceeds said

standard voltage, after said voltage applying section supplies said voltage in response to said first specifying signal supplied at said first timing.

9. (Original) The redundancy control circuit according to claim 8, wherein said timing setting section includes:

a first counter, which starts counting a first pulse number of said trigger signal when said first pulse number is N, and outputs a first control signal when counted said first pulse number is N,

a second counter, which starts counting a second pulse number of said trigger signal when said second pulse number is (M+N), and outputs a second control signal when counted said second pulse number is N, and

a third counter, which starts counting a third pulse number of said trigger signal when said third pulse number is (M+2xN), and outputs a third control signal when counted said third pulse number is N,

said first counter includes a first logical section which outputs a first said timing signal timing when said first specifying signal is outputted, based on an inversion signal of said second control signal and said first control signal, and

said second counter includes a second logical section which outputs a second timing signal indicative of a timing when said second specifying signal is outputted, based on an inversion signal of said third control signal and said second control signal.

10. (Previously Presented) The redundancy control circuit according to claim 1, wherein said program element is an anti-fuse.

11. (Currently Amended) A semiconductor memory, comprising:

a redundancy control circuit which includes:

a plurality of program elements, in which a defect address indicating a position of a defect is programmed by a dielectric breakdown due to applying of a voltage, and

a voltage control section which applies said voltage to part of a plurality of targeted program elements simultaneously, wherein said plurality of targeted program elements is part of said plurality of program elements to be dielectrically broken down correspondingly to said defect address;

one of a redundancy word line and a redundancy bit line which is replaced from one of a defective word line and a defective bit line corresponding to said defect address; and

a plurality of redundancy memory cells which is connected to one of said redundancy word line and said redundancy bit line;

wherein said voltage control section includes a timing setting section which outputs a timing signal indicating a timing for carrying out a dielectric breakdown of each of said plurality of program elements based on a trigger signal.

12. (Original) The semiconductor memory according to claim 11, wherein a number of said part of the plurality of targeted program elements, of which number is less than a number of said plurality of program elements, is one, and

said voltage control section applies said voltage to each of said plurality of targeted program elements, one by one.

13. (Original) The semiconductor memory according to claim 11, wherein said voltage control section applies said voltage to said plurality of targeted program elements, at a timing of a trigger signal.

14. (Currently Amended) The semiconductor memory according to claim 11, wherein:

said voltage control section commonly applies said voltage to said plurality of targeted program elements, and

said voltage is a voltage generated inside a device including said redundancy control circuit.

15. (Currently Amended) The semiconductor memory according to claim 11, wherein said voltage control section further includes:

~~a timing setting section which outputs a timing signal indicating a timing for carrying out a dielectric breakdown of each of said plurality of program elements based on a trigger signal, and~~

a plurality of element breakdown sections, each of which is installed correspondingly to said each of the plurality of program elements and applies said voltage to corresponding one of said plurality of program elements based on said timing signal and said defect address.

16. (Previously Presented) The semiconductor memory according to claim 15, wherein each of said plurality of element breakdown sections includes:

a fuse breakdown setting section which applies a specifying signal at a timing of said timing signal based on said defect address, wherein said specifying signal indicates whether or not said corresponding one of the plurality of program elements should be dielectrically broken down, and

a voltage applying section which applies said voltage to said corresponding one of the plurality of program elements in response to said specifying signal, when said specifying signal indicates that said corresponding one of the plurality of program elements should be dielectrically broken down.

17. (Original) The semiconductor memory according to claim 16, wherein a first timing is different from a second timing,

said first timing is a timing when a first said fuse breakdown setting section for a first one of said plurality of program elements, outputs a first said specifying signal, and

said second timing is a timing when a second said fuse breakdown setting section for a second one of said plurality of program elements, outputs a second said specifying signal.

18. (Previously Presented) The semiconductor memory according to claim 17, further comprising:

a comparing section which compares said voltage with a standard voltage and outputs a comparing result signal,

wherein said timing setting section generates said second timing based on said trigger signal and said comparing result signal indicating that said voltage exceeds said standard voltage, after said voltage applying section supplies said voltage in response to said first specifying signal supplied at said first timing.

19. (Original) The semiconductor memory according to claim 18, wherein said timing setting section includes:

a first counter, which starts counting a first pulse number of said trigger signal when said first pulse number is M, and outputs a first control signal when counted said first pulse number is N,

a second counter, which starts counting a second pulse number of said trigger signal when said second pulse number is (M+N), and outputs a second control signal when counted said second pulse number is N, and

a third counter, which starts counting a third pulse number of said trigger signal when said third pulse number is (M+2xN), and outputs a third control signal when counted said third pulse number is N,

said first counter includes a first logical section which outputs a first said timing signal indicative of a timing when said first specifying signal is outputted, based on an inversion signal of said second control and said first control signal, and

said second counter includes a second logical section which outputs a second timing signal indicative of a timing when said second specifying signal is outputted, based on an inversion signal of said third control signal and said second control signal.

20. (Previously Presented) The semiconductor memory according to claim 11, wherein said program element is an anti-fuse.

21. (Currently Amended) The semiconductor memory according to claim 11, wherein:

said semiconductor memory is DRAM, and

said plurality of program elements includes the same structure as a capacitor of a memory cell of said DRAM.